



## User and Programming manual

The MEGA mini-MPI is a four slot multipak interface for Tandy Color Computers. In addition to the usual cartridge slots and selection register, it includes a number of features not found on a standard MPI.

These include;

- Yamaha YMF262 (OPL3) sound chip
- 2 high speed UARTS (5v TTL)
- 3 programmable timers (two on the YMF chip)
- Source maskable IRQ system using FIRQ (/CART)
- Improved sound routing (software selectable source)

### **What an MPI is...**

An MPI or 'Multipack expansion interface' is how bus expansions are handled for the Color Computer line. These machines have a single cartridge expansion slot with most of the important signals found on a typical computer bus.

A multi-slot expansion can be plugged into the cartridge port, allowing multiple items to be connected at once, such as drive interfaces, serial ports, sound carts, ect. For multiple items to be connected to the system at once, some method of bus arbitration is needed so that different cartridges don't conflict with one another when using the bus.

This bus arbitration between slots is what lies at the heart of any multipak design. Two signals available at the cartridge port are used for this purpose, /CTS (cartridge select), and /SCS (spare chip select). These two signals are directed to a specific slot when the computer wants to access the cartridge in that slot. When the cart receives read and write requests for the addresses it uses AND one of these signals, it knows to respond.

The routing of these bus arbitration signals is controlled by the MPI register found at \$FF7F. This 8-bit register can be read or written by the system, and is laid out as follows.

REGISTER @ \$FF7F		CART* CTS*				SCS*				
DECIMAL	BIT	7	6	5	4	3	2	1	0	
0		0	0	0	0	0	0	0	0	- SLOT 1 SELECTED
17		0	0	0	1	0	0	0	1	- SLOT 2 SELECTED
34		0	0	1	0	0	0	1	0	- SLOT 3 SELECTED
51		0	0	1	1	0	0	1	1	- SLOT 4 SELECTED

If you're familiar with binary, you can see that this scheme supports up to 16 slots, with separate routing of /CTS and /SCS to each slot.

In the MEGA mini, the additional built in hardware items are accessed using this same arbitration. As if they were connected to a 'virtual slot'. For instance the MPI register would be set as follows;

<u>FEATURE</u>	<u>SIGNAL USED</u>	<u>VIRTUAL SLOT</u>
YMF262 (OPL3) sound chip	/SCS	5
Serial UARTS	/SCS	6
Additional MPI registers	/SCS	16

Details on what addresses are used for these items will be found under their own section further on in this manual. To use them first SCS must be set for the appropriate virtual slot in the MPI register (\$FF7F).

### **YMF262 (OPL3) sound chip**

The MEGA mini includes a Yamaha YMF-262 sound generator (OPL3), adding FM synthesis sound to the computer. This is the same sound chip used in several Soundblaster and AdLib sound cards for PCs in the past, and provides a whole new level of sound capability on the CoCo.

A low level stereo output is provided on the port side of the MEGA mini. This is the output that should be used for highest quality audio. It is suitable for connection only to an amplified output device, such as powered speakers or headphones, or an auxiliary input on an audio system or display. It won't drive non-amplified headphones or speakers.

The audio is also output on a single (mixed) channel to the cartridge port when selected via software controlled analog switch. This allows for output through the RF modulator or composite mod audio jacks, and may be used along with the low level audio jack on the unit.

Addresses for the YMF262 are gated with /SCS at virtual slot #5 (\$FF7F @ xxxx 0100).

<u>ADDRESS</u>	<u>DESCRIPTION</u>
\$FF50	PORT 0 - REG SELECT
\$FF51	PORT 0 - DATA
\$FF52	PORT 1 - REG SELECT
\$FF53	PORT 1 - DATA
\$FF54	YMF262 - RESET

The YMF262 has two sets of registers for specifying sounds. Registers in register array 0 are set by first writing the register number to \$FF50, and then writing the register value to the data port at \$FF51. For register array 1, use \$FF52 and \$FF53.

The registers in the YMF262 are write only, with the exception of the status register, which is read only (\$FF50), and provides the status of the chip's timer interrupts. Reading or writing \$FF54 performs a reset of chip registers, referred to as 'initial clear' in the data sheet.

Please refer to the programming section for information on the chip registers and their operation.

**Serial UARTS - SC16C550B (x2)**

The MEGA mini MPI includes two high-speed serial UARTs, taking the CoCo to a new level of performance in serial communications. Care has been taken to provide a full implementation, with all standard baud rates supported. The UARTs have been clocked so as to support the entire range of standard baud rates with a 0% baud rate error. Supported standard baud rates and the divisors to be used in initializing the UARTs are as follows;

<b><u>MEGA mini MPI UART baud rates</u></b>	
UART clock:	29.4912MHz
	29491200
<u>Divisor</u>	<u>Baud rate</u>
3072	600
1536	1200
768	2400
384	4800
192	9600
96	19200
48	38400
32	57600
16	115200
8	230400
4	460800
2	921600
1	1843200

Addresses \$FFx0 through \$FFx7 access the UART registers as detailed in the manufacturer data sheet. Reading or writing \$FFx8 performs a reset of the UART in question. This resets most registers in the UART. The specific effects of this reset can be found in the manufacturer data sheet.

The secondary data port at \$FFxA mirrors the THR/RHR registers at \$FFx0 and is included to aid in code optimization on the 6809 when using the UARTs in interrupt mode. This addition allows for the use of 16-bit reads and writes using the CPU's 'D' register. When using the the Hitachi 6309, the TFM instruction should instead be used with \$FFx0 instead.

Addresses for the UARTS are gated with /SCS at virtual slot #6 (\$FF7F @ xxxx 0101) as follows;

<u>ADDRESS</u>	<u>DESCRIPTION</u>
\$FF40	UART A - THR/RHR
\$FF41	UART A - IER
\$FF42	UART A - FCR/ISR
\$FF43	UART A - LCR
\$FF44	UART A - MCR
\$FF45	UART A - LSR
\$FF46	UART A - MSR
\$FF47	UART A - SPR
\$FF48	UART A - RESET
\$FF4A	UART A - SECONDARY DATA PORT, 16-BIT (MSB)
\$FF4B	UART A - SECONDARY DATA PORT, 16-BIT (LSB)
\$FF50	UART B - THR/RHR
\$FF51	UART B - IER
\$FF52	UART B - FCR/ISR
\$FF53	UART B - LCR
\$FF54	UART B - MCR
\$FF55	UART B - LSR
\$FF56	UART B - MSR
\$FF57	UART B - SPR
\$FF58	UART B - RESET
\$FF5A	UART B - SECONDARY DATA PORT, 16-BIT (MSB)
\$FF5B	UART B - SECONDARY DATA PORT, 16-BIT (LSB)

The physical I/O port for the UARTs consists of a 26-pin header found on the right side of the MEGA mini. This header provides access to all port-side UART signals, as well as +3.3V and +5V power. Pinout details are as follows;

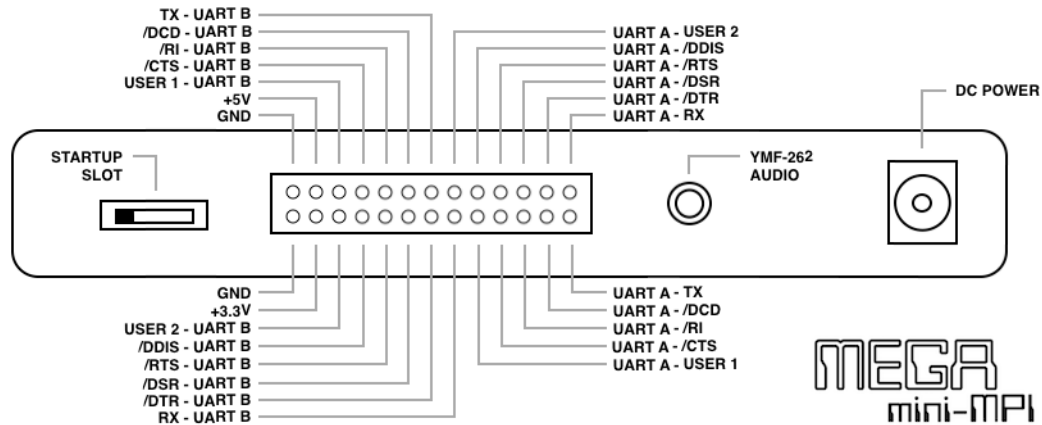


Figure 1

### **Extended MPI features**

The extended MPI features on the MEGA-mini include;

- an enhanced IRQ management system
- separate, selectable sound sources for cart port sound
- a programmable timer

Addresses for the MPI extended features are gated with /SCS at virtual slot #16 (\$FF7F @ xxxx 1111).

<u>ADDRESS</u>	<u>DESCRIPTION</u>
\$FF40	IRQ CONTROL REGISTER
\$FF41	ACTIVE IRQS
\$FF42	EXTENDED FEATURES REGISTER
\$FF43	TIMER MSB
\$FF44	TIMER LSB
\$FF45	TIMER RESET

### Enhanced IRQ management

The original MPI system provided a 6809 fast interrupt (the CART signal) which is routed to the slot currently tied to /CTS by the MPI register settings. This traditionally has been used to trigger execution of autostart ROM paks by simply connecting the Q clock to this interrupt.

In order to make this interrupt more useful, I've implemented an enhanced IRQ management scheme in the MEGA-mini which can be enabled and used by software. At startup, behavior of the CART line is as found in a standard MPI, but by setting a bit in the extended features register, enhanced IRQ handling can be enabled. This system also allows multiple cartridge devices to trigger an interrupt, whether the CART signal is currently routed to their slot or not.

Software must first change the CART interrupt vector in CoCo memory to execute an appropriate IRQ handling routine, set the IRQ control register, and then enable enhanced IRQ handling in the extended features register.

There are eight available interrupt sources on the MEGA-mini MPI; the four cartridge slots, the YMF262 chip, UART A, UART B, and the programmable timer.

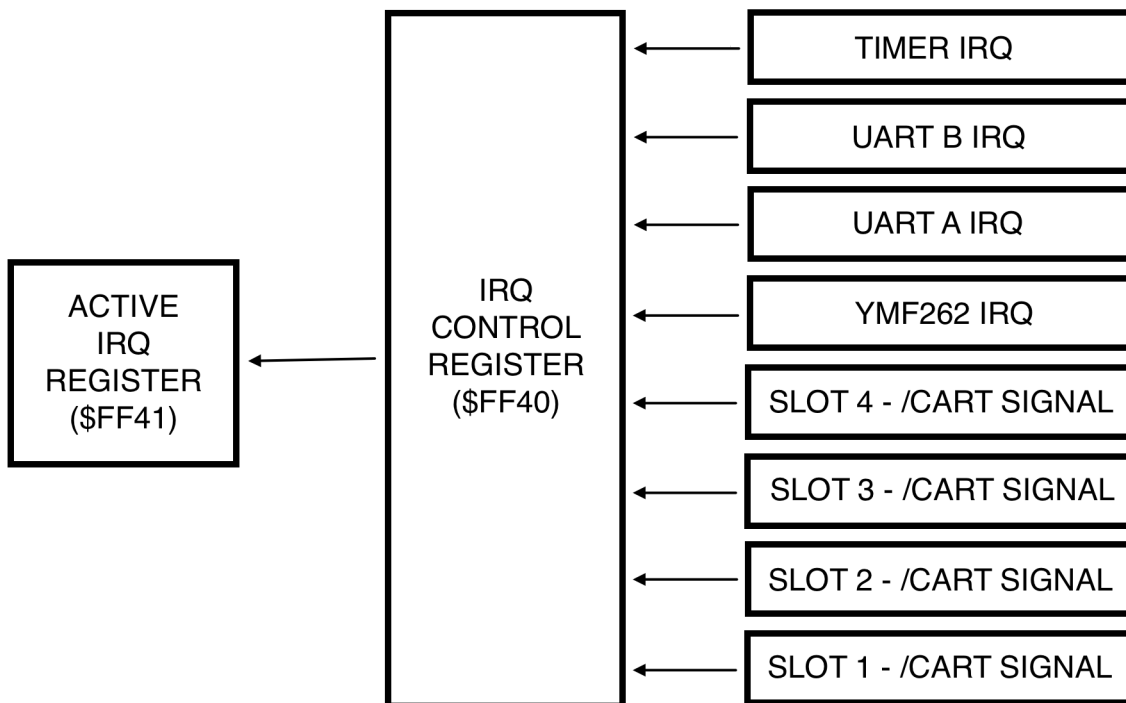


Figure 2

You specify to the system which interrupts you want enabled by setting bits in the IRQ control register. This 8-bit register can be both read from and written to, and is located at \$FF40 (slot 16). To enable an interrupt source, set it's bit to '1'.

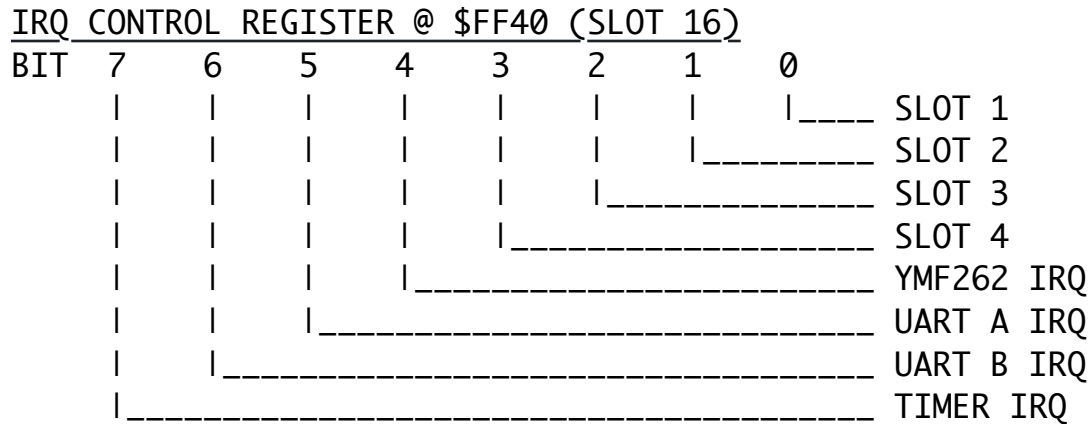


Figure 3

To enable the forwarding of the selected interrupts to the system, enable bit 7 of the extended features register located at \$FF42 (slot 16) - Figure 5. The three lowest bits of this register control sound source selection. This register may be both read and written as well.

Once the IRQ system is enabled, any interrupt occurring among the enabled sources will cause /CART to be asserted. Interrupt handling code can then read the IRQ status register at \$FF41 (slot 16) to determine the interrupt source(s) if more than one has been enabled. A set bit indicates an active interrupt signal.

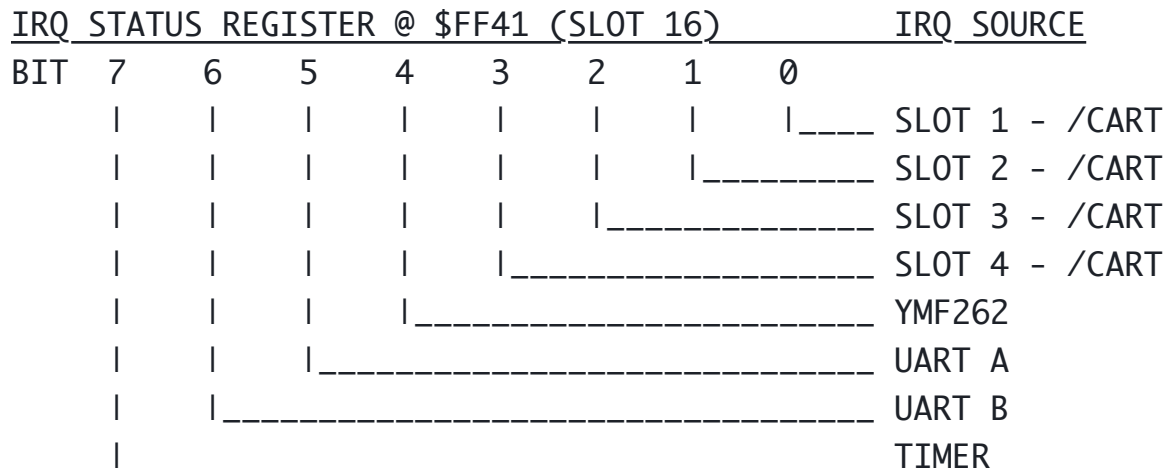


Figure 4



Sound source select (analog switch)

During development of the MEGA mini, it was discovered that multiple sound sources connected to the cart port sound\_in line adversely affects sound quality going back into the computer. This is remedied by the inclusion of an analog switch, which is used to select a single sound source to route to the cartridge port.

The lowest 3 bits of the extended features register select the sound source. At startup, the default selection is slot 1 (000). Sources and values are as follows;

EXTENDED REGISTER

<u>(2..0)</u>	<u>AUDIO SOURCE</u>
0 0 0	SLOT 1
0 0 1	SLOT 2
0 1 0	SLOT 3
0 1 1	SLOT 4
1 0 0	YMF-262
1 0 1	SLOT 1
1 1 0	SLOT 1
1 1 1	SLOT 1

EXTENDED MPI FEATURES REGISTER @ \$FF42 (SLOT 16)

BIT	7	6	5	4	3	2	1	0	
									ANALOG SWITCH A0
									ANALOG SWITCH A1
									ANALOG SWITCH A2
									NOT USED
									NOT USED
									NOT USED
									ENABLE TIMER
									ENABLE IRQ SYSTEM

Figure 5